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DRAWING AMENDMENTS

The attached sheet of drawings includes changes to Figs. 1 and 12. The labels, "self-test module", "interface circuit" (2 occurrences), and "terminal" (4 occurrences) have been added to Fig. 1. The labels, "test box", "wafer carriers", and "terminals" have been added to Fig. 12.

Attachments: 14 Replacement Sheets including 1 new drawing sheet

14 Annotated Sheets Showing Changes

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REMARKS

Reconsideration of the application is requested.

Claims 1-4 6-17, and 19-32 are now in the application. Claims 1-4, 6-17, 19-23, and 29-32 are subject to examination and claims 24-28 have been withdrawn from examination. Claims 31 and 32 have been added.

Under the heading "Drawings" on page 2 of the above-identified Office Action, the Examiner objected to the drawings. The Examiner stated that all rectangular boxes in Figs. 1 and 12 should be labeled. The Examiner also stated that the external testing device and the method steps should be shown.

Corrected drawings 1 and 12 have been provided in which all boxes have been labeled.

Please note that the external testing device is shown in Fig. 13.

New drawing Fig. 16 has been added to show the method steps. The specification has also been amended to describe the added figure. Support for the figure and the description can be found by referring to claims 1-10, for example.

Under the heading "Claim Rejections – 35 USC § 103" on page 4 of the above-identified Office Action, claims 1-4, 6, and 9-15 have been rejected as being

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obvious over U.S. Patent No. 6,651,202 to Phan in view of U.S. Patent No. 6,574,762 B1 to Karimi et al. under 35 U.S.C. § 103. Applicant respectfully traverses.

In attempting to equate the claimed invention to the prior art, the Examiner has not mentioned the teaching in Karimi et al. It therefore appears that the Examiner intended to reject the claims as being anticipated by U.S. Patent No. 6,651,202 to Phan, and the discussion below assumes that is in fact the case.

Claim 1 defines a method of testing an integrated circuit, which comprises:

> providing an integrated circuit that includes a self-test device;
>
> starting to perform a test of the integrated circuit with the self-test device;
>
> taking at least parts of the integrated circuit out of operation after the parts have been tested by the self-test device; and
>
> subsequently, connecting the integrated circuit to an external testing device that performs a function selected from the group consisting of reading out results of the test and evaluating the results of the test.

Claim 11 defines an apparatus for testing an integrated circuit using a self-test device that is located in the integrated circuit, which comprises:

> a self-test control device for causing testing of the integrated circuit by the self-test device before the integrated circuit is connected to an external testing device that performs a function selected from the group consisting of reading out results of the test and evaluating the results of the test;
>
> a test result memory located on the integrated circuit for storing the results of the test;

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an output circuit for forwarding the results stored in said test result memory to the external test device.

The Examiner has recognized that Phan does not teach that the BIST tests the memory array 100 before being connected to an external tester 160.

The Examiner, however, has stated that one can assume the BIST of Phan can operate to perform the self-test before being connected to the external tester 160. The Examiner has then stated that such a feature would have been a matter of design choice. Applicant disagrees with both statements.

The Examiner is correct in that Phan does teach that the testing by the BIST/BISR can be performed upon an initial power up or when initiated by the external ATE 160. This statement simply relates to the manner in which testing is started. It does not indicate anything related to whether or not the external ATE 160 is connected to the memory being tested.

More importantly, however, Phan specifically teaches that the external ATE 160 provides a clock signal FLARESCAN_IN_CLK to control the clocking of the BIST/BISR circuitry 122, and that other control signals are provided by the external ATE 160 (See column 8, lines 14-18).

Since the BIST circuitry 122 is controlled by a clock signal FLARESCAN_IN_CLK from the external ATE 160, it is clear that the external

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ATE 160 will be connected to the BIST circuitry 122 while the BIST circuitry 122 is performing testing.

Claim 3 specifies at least partially completing the test while performing a function selected from the group consisting of temporarily storing the integrated circuit and transporting the integrated circuit to the external testing device.

Claim 13 specifies that the self-test control device is configured to test the integrated circuit while allowing a function, selected from the group consisting of temporarily storing the integrated circuit and transporting the integrated circuit to the external testing device, to be performed.

The Examiner has referred to column 9, lines 44-64 to support the allegation that Phan teaches the limitations defined by claims 3 and 13. That portion of Phan only relates to the operation of the BIST/BISR circuitry 122 and to the application of stress factors to the integrated circuit under test. There is nothing that relates to temporary storage or to transporting the integrated circuit.

Support for added claims 31 and 32 can be found by referring to claims 3 and 13.

With regard to claims 31 and 32, Phan does not teach or suggest testing the integrated circuit with the BIST/BISR circuitry 122 while the integrated circuit is being transported.

Under the heading "Claim Rejections – 35 USC § 103" on page 6 of the above-identified Office Action, claims 7, 8, 16, 17, 19-23, 29, and 30 have been rejected as being obvious over U.S. Patent No. 6,651,202 to Phan in view of U.S. Patent No. 6,574,762 B1 to Karimi et al. under 35 U.S.C. § 103. Applicant respectfully traverses.

Claims 7-8 depend form claim 1, and therefore, even if there were a suggestion to combine the teachings for some reason, the invention as defined by claims 7 and 8 would not have been obtained for the reasons given above with regard to claim 1.

Claim 30 depends form claim 11, and therefore, even if there were a suggestion to combine the teachings for some reason, the invention as defined by claim 30 would not have been obtained for the reasons given above with regard to claim 11.

Additionally, please note that claim 7 refers to parts of the integrated circuit that have been tested (see claim 1). In contrast, Karimi et al. teach blocking the clock from the BIST 104, which has not been tested, but rather is the test device (See column 7, lines 53-57 and Fig. 1).

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Additionally with regard to claim 8 and also with regard to claim 29, please note that column 7, line 57 through column 8, line 12 of Karimi et al. does not teach anything related to discontinuing the supply voltage to take parts of the integrated circuit out of operation.

With regard to claim 16, the components are tested by a self-test device, and a device takes specific ones of said components (which are tested) out of operation, said device preventing a clock signal, needed to operate said components, from being applied to said specific ones of said components. In contrast, Karimi et al. teach blocking the clock from the BIST 104, which is not a component that has been tested, but rather is the test device.

Claims 17 and 19-23 are not obvious for the reasons specified above with regard to claim 16.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1, 11, 16, or 29. Claims 1, 11, 16, and 29 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent one of those independent claims.

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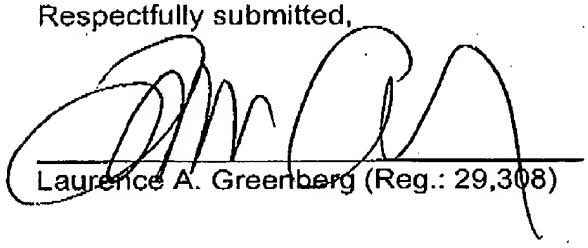
In view of the foregoing, reconsideration and allowance of claims 1-4, 6-17, 19-23, and 29-32 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

A fee in the amount of $100.00 has been enclosed for presenting two additional claims in excess of twenty.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,



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